

المُلَكَةُ الْغِزَائِيَّةُ السُّنُعُوْدِيَّةُ وُزَارِلَا النَّعَالِيْنَ جَمَامِحِ مُنْشَعَ قَبِرُكُ جَمَامِحِ مُنْشَعَ قَبِرُكُ (١٤٥)

(045)

## COLLEGE OF COMPUTING AND INFORMATION TECHNOLOGY

كلية الحاسب الآلي وتقنية المعلومات

Microprocessor and Assembly Language (301 اعلا)

#### **Course Description**

In this course, we will cover topics such as Machine organization; assembly language: addressing, stacks, argument passing, arithmetic operations, decisions, modularization; Input/Output Operations and Interrupts; Memory Hierarchy and Cache memory; Pipeline Design Techniques; Super scalar architecture; Parallel Architectures.

#### **Course Objective**

By the completion of the course the students should be able to

- 1. Ability to analyze, write, and test MIPS assembly language programs.
- 2. Ability to describe the organization and operation of integer and floating-point arithmetic units.
- 3. Ability to apply knowledge of mathematics in CPU performance analysis and in speedup computation.
- 4. Ability to design the datapath and control unit of a processor.
- 5. Ability to use simulator tools in the analysis of assembly language programs and in CPU design.

#### References

### Required:

David Patterson and John Hennessy. Computer Organization & Design:

The Hardware/Software Interface. Morgan Kaufmann Publishers, 2005(Third Edition)

#### Recommended:

Robert Britton. MIPS Assembly Language Programming. Pearson Prentice Hall, 2004

Prerequisite: Digital logic design (211 عال



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### **Evaluation Method:**

Method	Percentage
Quizzes & Assignments	10%
Lab	10%
Projects	10%
Test 1 & Test 2	30%
Final Examination	40%

Weeks	Topic Name	Sub Topic	Reading Chapter
1	Introduction	Introduction to computer architecture, assembly and machine languages, components of a computer system, memory hierarchy, instruction execution cycle, chip manufacturing process, technology trends, programmer's view of a computer system.	1&2
2	Review of Data Representation	Binary and hexadecimal numbers, signed integers, binary and hexadecimal addition and subtraction, carry and overflow, characters and ASCII table.	2.



المُلكَةُ الغَّرِّزِيَّةُ السُّنُعُوْدِيَّةُ وَزَارِةِ النَّعَلِيْمُ جَمَامِحِ مُرْشِيَّةً مِثَلَّةً جَمَامِحِ مُرْشِيَّةً مِثَلَّةً (١٤٥)

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Weeks	Topic Name	Sub Topic	Reading Chapter
3	Instruction Set Architecture	Instruction set design, RISC design principles, MIPS instructions and formats, registers, arithmetic instructions, bit manipulation, load and store instructions, byte ordering, jump and conditional branch instructions, addressing modes, pseudo instructions.	2
4	MIPS Assembly Language Programming	Assembly language tools, program template, directives, text, data, and stack segments, defining data, arrays, and strings, array indexing and traversal, translating expressions, if else statements, loops, indirect jump and jump table, console input and output.	2
5	Procedures and the Runtime Stack	Runtime stack and its applications, defining a procedure, procedure calls and return address, nested procedure calls, passing arguments in registers and on the stack, stack frames, value and reference parameters, saving and restoring registers, local variables on the stack.	4
6	Test 1		

**TECHNOLOGY** 



لَمُلُكَمَّةُ الْغَرِّنِيَّةُ السَّنُعُوْدِيِّةُ وزارة التَّعَلَيْمُ جَمَامِحَةُ مُنْ السَّعَالِمُّ جَمَامِحَةً مُنْ السَّعَالِةَ

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## (٠٤٥) كلية الحاسب الآلي وتقنية المعلومات

#### Weeks Sub Topic Reading Chapter **Topic Name** 7 **Interrupts** Software exceptions, syscall instruction, hardware interrupts, interrupt processing and handler, MIPS coprocessor 0. 8&9 Hardware adders, barrel shifter, 4 Integer Arithmetic and multifunction ALU design, integer ALU design multiplication, shift add multiplication hardware, Shiftsubtract division algorithm and hardware, MIPS integer multiply and divide instructions, HI and LO registers. 10 Floating-point 3 Floating-point representation, arithmetic IEEE 754 standard, FP addition and multiplication, rounding, MIPS floating-point coprocessor and instructions. CPU performance and metrics, 11 **CPU Performance** 4&7 CPI and performance equation, MIPS, Amdahl's law. 12 Test 2 13 Single-Cycle 4&7 Designing a processor, register transfer, datapath components, Datapath and Control Design register file design, clocking methodology, control signals,



لَمُلُكَةُ الْغَرِّنِيَّةُ السُّنُعُونِيِّةُ فِرْلِوَ النَّعَلِيْمُ جَمَامِ عَجُمُرُشِّ عَيْمِ الْفَ جَمَامِ عَجُمُرُشِ عَيْمَ الْفَالِقَ (٥٤٥)

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## كلية الحاسب الآلي وتقنية المعلومات

Weeks	Topic Name	Sub Topic	Reading Chapter
		implementing the control unit, estimating longest delay.	
14	Pipelined Datapath and Control	Pipelining concepts, timing and performance, 5-stage MIPS pipeline, pipelined datapath and control, pipeline hazards, data hazards and forwarding, control hazards, branch prediction.	4&7
15	Final Examination		